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Application No.	10/676,961
Filing Date	September 30, 2003
First Named Inventor	Florence R. Pon
Art Unit	2815
Examiner Name	Chris C. Chu
Attorney Docket Number	42P17605

Total Number of Pages in This Submission

19

ENCLOSURES (check all that apply)

☒ Fee Transmittal Form

☒ Fee Attached

☐ Amendment / Reply

☐ After Final

☐ Affidavits/declaration(s)

☐ Extension of Time Request

☐ Express Abandonment Request

☐ Information Disclosure Statement

☐ PTO/SB/08

☐ Certified Copy of Priority Document(s)

☐ Response to Missing Parts/Incomplete Application

☐ Basic Filing Fee

☐ Declaration/POA

☐ Response to Missing Parts under 37 CFR 1.52 or 1.53

☐ Drawing(s)

☐ Licensing-related Papers

☐ Petition

☐ Petition to Convert a Provisional Application

☐ Power of Attorney, Revocation Change of Correspondence Address

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☐ After Allowance Communication to TC

☐ Appeal Communication to Board of Appeals and Interferences

☒ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)

☐ Proprietary Information

☐ Status Letter

☐ Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name

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BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Signature

Date

November 16, 2006

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Tu T. Nguyen

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November 16, 2006



FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

Complete if Known

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☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$)

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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FEE CALCULATION

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051		2051		Surcharge - late filing fee or oath	
1052		2052		Surcharge - late provisional filing fee or cover sheet.	
2053		2053		Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) (\$)

SUBMITTED BY

Complete (if applicable)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No. : 10/676,961
Applicant : Florence R. Pon
Filed : 09/30/2003
TC/A.U. : 2815
Examiner : Chris C. Chu

Confirmation No. 8131

Docket No. : 042390.P17605
Customer No. : 8791

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants submit the following Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. In response to Notice of Non-Compliant Appeal Brief, Applicants have revised the claim status for the application on Appeal. Applicants have submitted a check number 833 in the amount of \$625.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §41.20(b) and one-month extension of time fee. Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666. A duplicate copy of the Fee Transmittal is enclosed for this purpose.

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-32 of the present application are pending. Claims 3-5 and 11-30 have been withdrawn and claims 1, 2, 6-10, 31 and 32 remain rejected. The Applicants hereby appeal the rejection of claims 1, 2, 6-10, 31 and 32.

IV. STATUS OF AMENDMENTS

The Applicants filed an amendment on February 27, 2006, in response to aa Office Action issued by the Examiner on December 29, 2005. In response to the February 27, 2006 amendment, the Examiner issued a Final Office Action on May 19, 2006. The Applicants filed a Notice of Appeal and a Pre-Appeal Brief Request for Review on August 7, 2006. The review panel issued a decision on September 15, 2006, stating that the application remains under appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Claims 1, 2, 6,-10, 31 and 32:

An embodiment of the present invention is a technique to stack dies in a die assembly. A plurality of dies are stacked on top of one another in a staggered configuration such that an upper die in a pair of adjacent dies face downward or upward and is displaced by a first distance with respect to a lower die in the pair. The adjacent dies are attached by an adhesive layer between the adjacent dies¹.

¹ Specification, paragraph [0014].

A package assembly 100 includes a substrate 110, a plurality of dies 120₁ to 120_N, a plurality of bond pads 130₁ to 130_K, and a plurality of conductors 140₁ to 140_M². Each of the dies has a number of bond pads 130_j's ($j = 1, \dots, K$) to provide contact for interconnections. When the bond pads are not suitably placed, a redistribution layer may be formed to redistribute the interconnection pattern³. The conductors 140_k's ($i = 1, \dots, M$) connect the bond pads from the dies to the bond pads on the substrate⁴.

The pair 120_k includes an upper die 122 and a lower die 125 and an adhesive layer 127⁵. The upper die 122 has four edges: upper first, second, third, and fourth edges. The upper first and third edges are opposite to each other and the upper second and fourth edges are opposite to each other⁶. Similarly, the lower die 125 has four edges: lower first, second, third, and fourth edges. The lower first and third edges are opposite to each other and the lower second and fourth edges are opposite to each other⁷.

The upper die 122 is stacked on top of the lower die 125 such that the upper first edge is displaced from the lower first edge by a first distance d_1 . The upper die 122 may also be displaced by any angle with respect to the lower die 125. The stacking may also be extended to the other dimension such that the upper second edge is displaced from the lower second edge by a second distance d_2 . The adhesive layer deposited between the upper and lower dies 122 and 125 to attach these two dies together⁸.

The upper die 122 and the lower die 125 may be stacked such that the bottom surface of the upper die 122 is attached to the top surface of the lower die 125⁹. The conductors are connected or attached to the bond pads of the dies. For example, upper conductor 142 is attached to the upper bond pad of the upper die 122 and lower conductor 144 is attached to the lower bond pad of the lower die 125. Since the dies are offset to each other by a distance, the upper conductor 142 and the lower conductor 144 are separated by a conductor distance¹⁰.

² Specification, paragraph [0018]; Figure 1A.

³ Specification, paragraph [0020], [0046]; Figure 6, block 620.

⁴ Specification, paragraph [0020].

⁵ Specification, paragraph [0023].

⁶ Specification, paragraph [0024]; Figure 1B.

⁷ Specification, paragraph [0025]; Figure 1B.

⁸ Specification, paragraph [0026].

⁹ Specification, paragraph [0027].

¹⁰ Specification, paragraph [0028].

As an illustrative example, a four-dice configuration is shown¹¹. The dies are offset in both directions or dimensions by distances d_1 and d_2 . The conductors connect the bond pads on both stair-case sides of each die to the bond pads of the substrate. The dies 120₂ and 120₄ face toward their respective lower dies, i.e., die 120₁ and 120₃, respectively. The conductors 140₂ and 140₄ are connected to the bond pads on the dies 120₂ and 120₄ facing downward¹².

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 2, 6-10, 31 and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,476,474 issued to Hung ("Hung") in view of U.S. Patent No. 5,998,864 issued to Khandros ("Khandros").

VII. ARGUMENTS

A. Claims 1, 2, 6-10, 31 and 32 Are Not Obvious over Hung in view of Khandros.

In the Final Office Action, the Examiner rejected claims 1, 2, 6-10, 31, and 32 under 35 U.S.C. §103(a) as being unpatentable over ("Hung") in view of U.S. Patent No. 5,998,864 issued to Khandros et al. ("Khandros"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a *prima facie* case of obviousness.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004)*. Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

¹¹ Specification, paragraphs [0030], [0033], and [0035]; Figures 2A, 2B, and 3.

¹² Specification, paragraph [0036]; Figure 3.

Hung discloses a dual-die package structure and method for fabricating the same. The attachment of the second die over the first die constitutes a face-to-face stacked dual die construction (Hung, col. 4, lines 8-9).

Khandros discloses a stacking semiconductor devices particularly memory chips. Each semiconductor device has a front surface and a back surface and the front surface of the devices 408, 406, and 404 are adjacent to the back surfaces of the semiconductor devices 406, 404, and 402, respectively (Khandros, col. 6, lines 44-49).

Hung and Khandros, taken alone or in any combination, do not disclose, suggest, or render obvious, at least one of (1) stacking an upper die having upper top and bottom surfaces and upper first, second, third, and fourth edges on top of a lower die having a lower top surface and lower first, second, third, and fourth edges such that the upper first edge is displaced from the lower first edge by a first distance, the upper first and third edges being opposite to each other, the lower first and third edges being opposite to each other, (2) the upper bottom surface facing toward the lower top surface such that bond pads on the upper die facing downward while bond pads on the lower die facing upward; (3) attaching the upper die to the lower die with an adhesive layer between the upper and lower dies; and (4) attaching the upper die to a third die such that the lower die, the upper die, and the third die are stacked in a stair-case configuration, as recited in claims 1 and 31; and (5) stacking a plurality of dies having at least three dies on top of one another in a staggered configuration such that an upper die top surface in a pair of adjacent dies faces downward or upward and is displaced by a first distance with respect to a lower die in the pair.

Hung merely discloses a dual-die packaging involving exactly two dies facing each other. Since there are only two dies, there cannot be a staggered arrangement as recited in claims 1 and 31. The dual-die arrangement in Hung cannot be expanded to more than two dies because the bonding wires 410 and 420 connected to the conductive leads 310 and 320 respectively, prevent additional wires to connect a third die to the conductive leads 310 or 320. The two conductive leads 310 and 320 are positioned on both sides of the dies, and not at the bottom of the dies as in the present invention. This configuration limits the interconnection patterns to only two dies.

In addition, Hung does not disclose a redistribution layer as recited in claims 7 and 17. The Examiner states that inherently, the circuit surfaces (100a and 200a) in the upper

9200) and lower (100) dice contain a circuit layer that provides electrical connections between the bond pads (110 and 210) and internal elements inside of the upper (200) and lower 9100) die (Final Office Action, page 9, lines 2-5). The Examiner then concludes that this circuit layer of Hung reads as a redistribution layer (Final Office Action, page 9, line 5). However, Hung merely discloses that the die is formed with a lined array of bond pads on one edge (Hung, col. 3, lines 43-47). A lined array of bond pads is not the same as a redistribution layer.

Khandros merely discloses the front surface of the devices 408, 406, and 404 face the back surfaces of the semiconductor devices 406, 404, and 402, respectively (Khandros, col. 6, lines 44-49). Therefore, all semiconductor devices face in the same direction so that all the bond pads 412, 414, 416, and 418 are disposed along a common edge of the semiconductor devices (Khandros, col. 6, lines 51-54). In contrast, the claimed invention provides for the upper bottom surface facing toward the lower top surface such that bond pads on the upper die facing downward while bond pads on the lower die facing upward.

In the Final Office Action, the Examiner contends that Khandros does not have to teach “the upper bottom surface facing toward the lower top surface such that bond pads on the upper die facing downward while bond pads on the lower die facing upward.” (Final Office Action, page 9, lines 16-18). However, without this teaching, Khandros cannot be combined with Hung. In fact, the fact that Hung did not extend Khandros teaching to include this aspect indicates that it was not obvious at the time to combine the two references.

Hung does not disclose or suggest a stair-case configuration extending to more than two dies because of the manner in which the bonding wires are connected to the conductive leads. Khandros does not disclose or suggest the bond pads facing each other. Accordingly, they cannot be combined.

There is no motivation to combine Hung and Khandros because neither of them addresses the problem of spacer-less die stacking. There is no teaching or suggestion that a staggered arrangement or a staircase configuration is present. Hung, read as a whole, does not suggest the desirability of staggering the dies. For the above reasons, the rejection under 35 U.S.C. §103(a) is improperly made.

When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be

considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Col, Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). “When determining the patentability of a claimed invention which combined two known elements, ‘the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.’” In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. “To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.” Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Furthermore, although a prior art device “may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so.” In re Mills 916 F.2d at 682, 16 USPQ2d at 1432; In re Fitch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992).

In the present invention, the cited references do not expressly or implicitly suggest a staggered arrangement. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Hung and Khandros is an obvious application of spacer-less die stacking.

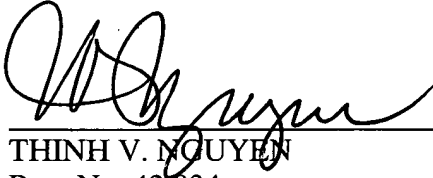
Therefore, Applicants believe that independent claims 1 and 31 and their respective dependent claims are distinguishable over the cited prior art references.

VIII. CONCLUSION

Applicant respectfully requests that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated nor rendered obvious by the prior art.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

A handwritten signature in black ink, appearing to read 'Thinh V. Nguyen', is written over a horizontal line.

THINH V. NGUYEN
Reg. No. 42,034

Dated: November 16, 2006

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IX. CLAIMS APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (previously presented) A method comprising:

stacking an upper die having upper top and bottom surfaces and upper first, second, third, and fourth edges on top of a lower die having a lower top surface and lower first, second, third, and fourth edges such that the upper first edge is displaced from the lower first edge by a first distance, the upper first and third edges being opposite to each other, the lower first and third edges being opposite to each other, the upper bottom surface facing toward the lower top surface such that bond pads on the upper die facing downward while bond pads on the lower die facing upward;

attaching the upper die to the lower die with an adhesive layer between the upper and lower dies; and

attaching the upper die to a third die such that the lower die, the upper die, and the third die are stacked in a stair-case configuration.

2. (previously presented) The method of claim 1 further comprising:

attaching upper and lower conductors to upper and lower bond pads of the upper and lower dies at the upper and lower first edges, respectively, such that the upper and lower conductors are separated by a conductor distance.

3. (withdrawn) The method of claim 1 further comprising:

attaching upper and lower conductors to upper and lower bond pads of the first and second dies at the upper third and the lower first edges, respectively.

4. (withdrawn) The method of claim 1 wherein stacking the upper die comprises:

stacking the upper die on top of the second die such that the upper second edge is displaced from the lower second edge by a second distance.

5. (withdrawn) The method of claim 4 further comprising:

attaching upper and lower conductors to upper and lower bond pads of the upper and lower dies at the upper and lower second edges, respectively, such that the upper and lower conductors are separated by a conductor distance.

6. (original) The method of claim 1 further comprising:
attaching the lower die to a substrate by a second adhesive layer deposited between the lower die and the substrate.

7. (original) The method of claim 1 further comprising:
depositing an upper redistribution layer to place bond pads on the upper die.

8. (original) The method of claim 7 further comprising:
depositing a lower redistribution layer to place bond pads on the lower die.

9. (original) The method of claim 1 wherein stacking the upper die comprises:
stacking the upper die on top of the lower die, the upper and lower die having same or substantially similar sizes.

10. (original) The method of claim 1 wherein attaching comprises:
attaching the upper die to the lower die by the first adhesive layer made of a non-conductive or conductive material.

11. (withdrawn) A method comprising:
stacking a plurality of dies having at least three dies on top of one another in a staggered configuration such that an upper die top surface in a pair of adjacent dies faces downward or upward and is displaced by a first distance with respect to a lower die in the pair; and

attaching the adjacent dies by an adhesive layer between the adjacent dies.

12. (withdrawn) The method of claim 11 further comprising:
attaching conductors to bond pads of the adjacent dies such that the conductors are separated by a conductor distance.

13. (withdrawn) The method of claim 11 wherein stacking comprises:
stacking the plurality of dies in a first stair-case configuration in a first dimension.
14. (withdrawn) The method of claim 13 wherein stacking further comprises:
stacking the plurality of dies in a second stair-case configuration in a second
dimension.
15. (withdrawn) The method of claim 11 wherein stacking comprises:
stacking the plurality of dies in a first alternate staggering configuration in a first
dimension.
16. (withdrawn) The method of claim 15 wherein stacking further comprises:
stacking the plurality of dies in a second staggering configuration in a second
dimension.
17. (withdrawn) The method of claim 11 further comprising:
depositing a redistribution layer to place bond pads on at least one of the plurality
of the-dies.
18. (withdrawn) The method of claim 11 wherein stacking comprises:
stacking the plurality of dies having same or substantially similar sizes.
19. (withdrawn) The method of claim 11 wherein stacking comprises:
stacking the plurality of dies on top of a substrate; and
attaching a bottom die of the plurality of dies to the substrate by an adhesive.
20. (withdrawn) The method of claim 11 wherein attaching comprises:
attaching the adjacent dies by the adhesive layer made of a non-conductive or
conductive material.
21. (withdrawn) A die assembly comprising:

a plurality of dies stacked on top of one another in a staggering configuration such that an upper die top surface in a pair of adjacent dies faces downward or upward and is displaced by a first distance with respect to a lower die in the pair; and

an adhesive layer between the adjacent dies to attach the adjacent dies.

22. (withdrawn) The die assembly of claim 21 further comprising:
conductors attached to bond pads of the adjacent dies such that the conductors are separated by a conductor distance.

23. (withdrawn) The die assembly of claim 21 wherein the plurality of dies are stacked in a first stair-case configuration in a first dimension.

24. (withdrawn) The die assembly of claim 23 wherein the plurality of dies are stacked in a second stair-case configuration in a second dimension.

25. (withdrawn) The die assembly of claim 21 wherein the plurality of dies are stacked in a first alternate staggering configuration in a first dimension.

26. (withdrawn) The die assembly of claim 25 wherein the plurality of dies are stacked in a second staggering configuration in a second dimension.

27. (withdrawn) The die assembly of claim 21 further comprising:
a redistribution layer to place bond pads on at least one of the plurality of the dies.

28. (withdrawn) The die assembly of claim 21 wherein the plurality of dies having same or substantially similar sizes.

29. (withdrawn) The die assembly of claim 21 further comprising:
a substrate attached to a bottom die of the plurality of dies by an adhesive.

30. (withdrawn) The die assembly of claim 21 wherein the adhesive layer is made of a non-conductive or conductive material.

31. (previously presented) A method comprising:

stacking an upper die having upper top and bottom surfaces and upper first, second, third, and fourth edges on top of a lower die having a lower top surface and lower first, second, third, and fourth edges such that the upper first edge is displaced from the lower first edge by a first distance, the upper first and third edges being opposite to each other, the lower first and third edges being opposite to each other, and such that bond pads on the upper die facing downward while bond pads on the lower die facing upward;

attaching the upper die to the lower die with an adhesive layer between the upper and lower dies;

attaching upper and lower conductors to upper and lower bond pads of the upper and lower dies at the upper and lower first edges, respectively, such that the upper and lower conductors are separated by a conductor distance; and

attaching the upper die to a third die such that the lower die, the upper die, and the third die are stacked in a stair-case configuration.

32. (previously presented) The method of claim 31 wherein stacking comprises:

stacking the upper die such that the upper top surface or the upper bottom surface faces the lower top surface.

X. EVIDENCE APPENDIX

None

XI. RELATED PROCEEDINGS APPENDIX

There are no decisions rendered by a court of the Board in any proceedings which may be related to, directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal, as indicated in Section II (Related Appeals and Interferences).